Applicability of Cyclic-Memory Networks and IEEE1394 for Fine Motion Control and Arcade Games

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Abstract

Motion control and arcade games require a high bandwidth and periodic transfers to meet the needs of more precise control of motors, and more players and more complex graphics in arcade games. There is a common-memory architecture called "Cyclic Memory" because the data is refreshed periodically, which is well known in the field of real-time systems. IEEE1394 has been drawing considerable attention as the need for connecting audio/visual electronics with a unified fast interface increases. We discuss the feasibility of Cyclic Memory on the IEEE1394 with its Isochronous mode. By analyzing the requirements of two prototypical applications, we evaluate the performance and other capabilities of IEEE1394 and the other networks that have the functionality of Cyclic Memory, and discuss their applicability. We also discuss the network reliability based on IEEE1394 when it is applied to an actual motion control system.

1. Introduction

In the field of motion control, there is an increasing need of precise control of motors for transporting materials and products. For example, PCB (Printed Circuit Board) manufacturing requires a sampling period shorter than 1 msec to make more precise small holes on the boards and to enhance productivity. Although there has been a conventional way of direct control with DI (Digital Input) / DO (Digital Output) modules and controllers, it may not satisfy the required performance because the latency of I/O modules is very high. The same can be said in arcade games. Recent rapid growth in the market of competing games, such as drive games, has pushed up the number of concurrent players. 16 to 32 players must be allowed to play together in the near future although at most 2 to 4 players are allowed to play nowadays. In this application, another requirement is to realize truly real graphics and motions of the cars. These requirements result in much more information to be exchanged among the game machines, that is, a higher bandwidth is needed. Game machine vendors have built multi-player systems with their own proprietary bus connecting machines together, whose baud rate is around 10 Mbps, but it turns out to be insufficient to meet the application requirement of high bandwidth.

In order to deal with this problem, we investigate the capabilities of several networks to realize a common-memory architecture called "Cyclic Memory" in which all nodes share information, and discuss their applicability. In the Cyclic-Memory architecture, every node changes turn to send all of its own data which is then received by the others simultaneously. On the other hand, there is another way called "Reflective Memory" which performs the same function as Cyclic Memory. But it differs from the Cyclic Memory in terms of the method of copying memory: it only broadcasts just-written data in the memory area. Due to its efficiency of copying memory, the Reflective Memory has been considered for aircraft simulators [1] and reported to be used for an actual simulator system [2]. It has good performance with a unique way of copying memory but it requires some specific hardware to detect the change of data. By contrast, the Cyclic Memory doesn't require such hardware.

There have already been various products in the market that have the functionality of Cyclic Memory, and we consider Ethernet and FDDI (Fiber Distributed Data Interface) based systems as examples of these. The conventional Ethernet can't meet real-time requirements because under its MAC (Medium Access Control) layer, CSMA/CD protocol, any node can access the bus as soon as the bus becomes free. To cope with this problem, some methods have been proposed to modify MAC layer [3], transport layer [4], and add some specific protocol between transport and application layers [5]. FDDI is a token-passing protocol guaranteeing that every node on the ring can send its data within a specific time. Furthermore, we also consider IEEE1394 due to its high bandwidth up to 400 Mbps and its original Isochronous mode, which assures fair arbitration for all nodes on the bus and periodic data transfers.

2. Feasibility of Cyclic Memory with IEEE1394

Figure 1 illustrates the basic idea of Cyclic Memory with three nodes A, B, and C on a network. Every node has the same amount of common memory that consists of a number of areas corresponding to the number of nodes. The memory has an area called the "transmission area" on which the node can write its own data and the other two areas called the "reception area" from which it can read data of the other nodes. Every node changes turn to broadcast the data of its transmission area, and it is copied to the corresponding reception area in the other nodes.

Figure 2 shows the details of IEEE1394 protocol. It originally has a specific cycle time, 125 μ sec, during which periodic data transfers can be performed. There are two parts of the cycle: "Isochronous mode" and "Asynchronous mode". The Isochronous mode is broadcast communication and suitable for periodic data transfers. The Asynchronous mode is appropriate for message transfer with handshaking [6], [7].

The Isochronous transfers with *a priori* assigned channel numbers and bandwidth can be broadcast over the bus, and one or more nodes can receive them simultaneously. For each node, however, these Isochronous transfers are supposed to be unidirectional, not bidirectional, because they are specified in advance by an application program as Isochronous transmission or Isochronous reception. Since the Cyclic Memory requires bidirectional communication for all nodes, it turns out to be impossible to perform the Cyclic Memory function with the Isochronous mode of IEEE1394.
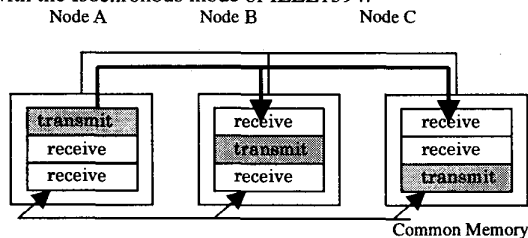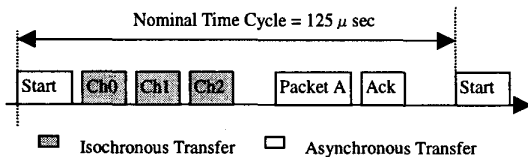

Figure 1.   The concept of Cyclic Memory

Figure 2.   IEEE1394 protocol

3. Analysis of Application Requirements

Motion control is generally used in a manufacturing system to transport materials and products. It essentially requires master-slave communication such that AC servo amplifiers which actuate motors are controlled by independent operational commands from a controller in terms of displacement, velocity, and torque. Consequently, each amplifier returns its current status to the controller. It suggests that the Cyclic Memory, in which all nodes essentially share all information, could be applied but might be more than enough because it just requires all amplifiers to have sufficient memory to save control commands. On the other hand, IEEE1394 is more suitable because returning status, which is a unidirectional communication, can be supported by the Isochronous mode and the command transfer by the Asynchronous mode with its point-to-point feature. In the field of PCB manufacturing, the sampling period is required to be around 100 μ sec so that one can make more precise small holes on the boards, thus enhancing productivity. To estimate the required bandwidth, assume that both 16 bytes for the control command and 16 bytes for the returned status are to be transferred for each node, the number of nodes is 32, and the period is 100 μ sec. Then we can estimate the bandwidth as:

$$32 \times (16 + 16) \text{ bytes} / 100 \,\mu \text{ sec} = 1024 \text{ bytes} / 100 \,\mu \text{ sec}$$
$$= 10.24 \text{ Mbytes} / \text{sec}$$

Although the inter-node distance depends upon the underlying motion control application, 10 to 20 meters would be sufficient, and any of bus, daisy chain, and ring can be used as its topology. The memory requirement doesn't seem to be high because 1024 bytes of memory would be sufficient, i.e., 32 nodes and 32 bytes per node.

Drive games, as an example of arcade games, allow several players to compete with each other, so it is required that any player can always check the other players' positions and motions in his playing window. This implies that the Cyclic Memory could be adapted to this application thanks to its feature of common memory. Then, IEEE1394 might not be applicable because it isn't appropriate for realizing the common memory. According to the need of increasing number of concurrent players and more sophisticated graphics, 16 to 32 players must be allowed to play in the near future although at most 2 to 4 players are allowed nowadays, and the memory size should be as much as a few kilobytes for each node. To estimate the bandwidth, assume that the typical memory size is 2Kbytes, the number of nodes is 32, and the period is 16.6 ms because this application has to show 60 frames per second. Then we compute the required bandwidth as:

$$32 \times 2 \text{ Kbytes} / 16.6 \text{ msec} = 64 \text{ Kbytes} / 16.6 \text{ msec}$$
$$= 3.85 \text{ Mbytes} / \text{sec}$$

The inter-node distance in drive games can be as short as a few meters because any player sits next to the others. That would naturally let the topology of this application be a bus or daisy chain, but a ring could also be used. The

required memory is larger than that of the motion control because it needs 64 Kbytes for each node, i.e., 32 nodes and 2 Kbytes per node.

4. Comparison of Network Performance and Capabilities

Table 1 shows a comparative perspective of Cyclic-Memory networks including Ethernet (FL-net: multi-vendor), FDDI (μ Σ-100: Hitachi), and IEEE1394, in order to contrast their performance and other capabilities.

FL-net, which has been standardized by the FA (Factory Automation) Control Network Committee of Japanese Manufacturing Science and Technology Center (JMSTC), is a network based on Ethernet to connect programmable, robot, and numerical controllers in manufacturing systems [5]. It performs the Cyclic Memory according to the token-passing scheme realized by a specific protocol called "FA link protocol" sitting between the transport and application layers. μ Σ-100 is one of Hitachi's control network products using FDDI which satisfies the needs of high performance, wide-area capability, and high reliability in large process systems. It also supports the Cyclic Memory with the conventional token-passing scheme of FDDI [8].

First, the available baud rate of the FL-net is defined as 10 Mbps, and the segment length can be extended up to 100, 185, and 500 meters for 10BASET, 10BASE2, and 10BASE5, respectively. Its topology comes in the form of a bus or star with a hub. The performance of FL-net is based upon the proposal by Japanese Automobile Manufacturers Association that each of 32 nodes sends 136 bytes of data where the period should be 50 ms, meaning that the bandwidth will be 0.086 Mbytes per second. Although FL-net defines up to 254 nodes attachable to the network, its performance will, of course, decrease as the number of nodes increases with a growing token-handling overhead. As seen from the table, the performance is the worst among the three due to the fact that it relies on FA link protocol software to handle token-passing schemes to realize Cyclic Memory. The required memory is relatively small because each node needs to transfer data up to a few hundred bytes. Ethernet is the cheapest due to its simple hardware and wide deployment in personal computers and many other peripherals.

Second, using FDDI, μ Σ-100 has the available baud rate up to 100 Mbps, and the segment length extends to 2000 meters, the longest among the three, which meets the requirement of vast chemical, steel and gas processing plants. Its topology is essentially a ring. The performance of μ Σ-100 is guaranteed when 32 nodes send a total of 40.96 Kbytes in a period of 20 msec, and hence the bandwidth will be as much as 2.048 Mbytes per second. Its memory requirement is the largest because some large

plants require a few hundred kilo bytes each. However, FDDI is the most expensive among the three.

For IEEE1394, the available baud rates are 100, 200, and 400Mbps, and the segment length can be as long as 100 meters with optical fiber cables, and 4.5 meters with shielded twisted pair cables that are relatively shorter than the other two networks. Its topology can be a daisy chain, tree, and a star due to its original aim of connecting home electronic appliances. Although it turns out that IEEE1394 doesn't support the Cyclic Memory as discussed in Section 2, its performance can be 4.5 Kbytes/125 μ s at maximum under the assumption that 32 nodes on the network perform Isochronous communication at 400 Mbps, and hence the bandwidth will be as much as 36 Mbytes per second. Isochronous gaps, which are timing gaps for arbitration, are also taken into consideration to derive this result. Such a good performance can be achieved by the DMA controller equipped in the Link layer LSI without any additional software. This is the point that makes the performance of IEEE1394 different from the other two networks. The amount of memory is secured by an application program according to its need. Its cost would be at the middle because the hardware is simple consisting of two LSIs, and their price decreases as their demand as home appliances increases.

Table 1. Comparative table of performance and capabilities

Network	Ethernet	FDDI	IEEE1394
	FL-net	μ Σ-100	
Baud rate(Mbps)	10	100	100,200,400
Performance @ 32nodes	4.3Kbytes/50ms (0.086Mbytes/s)	40.96Kbytes /20ms (2.048Mbytes/s)	4.5Kbytes /125 μ s (36Mbytes/s)
Segment length (m)	100 (10BASET) 185(10BASE2) 500(10BASE5)	2000	100(optical), 4.5(electric)
Network topology	bus, star with hub	ring	daisy chain, tree, star
Max.number of nodes	254	64	64
Amount of Memory (Kbytes)	17	256	As needed
Cable	100 Ω coaxial cable, 50 Ω category 3 unshielded cable,	optical fiber	optical fiber, shielded twisted pair
Cost	Cheapest	Most expensive	Middle

5. Evaluation of IEEE1394 network reliability

Recent PCB manufacturing systems require much higher reliability to reduce down times and enhance productivity. When applying an IEEE1394-based network

to it, we found a problem: if one intermediate node fails, the network communication would be separated into two or more parts because it takes a daisy chain, tree, or a star topology. This separation makes no sense to motion control because it can't send commands to all other nodes correctly. Therefore, we propose a dual IEEE1394 network system where each node is connected together with two current and standby networks.

We now discuss the reliability of the dual network and compare it with a single one. There are three components in an IEEE1394 network interface: the Link layer LSI, the Physical layer LSI, and the connectors. The main factors that might bring the whole single network down consist of a breakdown of the Link layer LSI in the Cycle Master node, that of the Physical layer LSI, and that of the connectors, because they will all cause fatal communication errors. Hence, assuming that every component failure follows an exponential process with rate λ_{lin}, λ_{phy}, and λ_{con}, respectively, we can describe the reliability of the single network, $R_{single}(t)$, as:

$$R_{single}(t) = \exp\left(-(\lambda_{lin} + \lambda_{phy} + \lambda_{con}) \cdot t\right)$$
$$= \exp(-\lambda_{sys} \cdot t)$$

where $\lambda_{sys} = \lambda_{lin} + \lambda_{phy} + \lambda_{con}$ is the single system failure rate. On the other hand, considering that the dual network comprises two single networks, its reliability, $R_{dual}(t)$, can be written as:

$$R_{dual}(t) = 1.0 - \prod_{i=1}^{2}(1.0 - R_{single,i}(t))$$
$$= 2 \cdot \exp(-\lambda_{sys} \cdot t) - \exp(-2 \cdot \lambda_{sys} \cdot t)$$

Now, assume that the failure rates of the Link layer LSI, the Physical layer LSI, and the connectors are 200×10^{-9}, 150×10^{-9}, and 50×10^{-9} failures per hour, respectively. Furthermore, assume that one fifth of the Link layer LSI logic contributes to generating the Cycle Start packet that is essential to the timing management, one third of the Physical layer LSI logic takes part in repeating the incoming signal to the other ports, and the probability of an intermittent failure of the connectors is 0.01. Then the actual failure rates λ_{lin}, λ_{phy}, and λ_{con} bringing the entire single network down are:

$$\lambda_{lin} = (200 \times 10^{-9}) / 5 = 40 \times 10^{-9} \text{ failures per hour}$$

$$\lambda_{phy} = (150 \times 10^{-9}) / 3 = 50 \times 10^{-9} \text{ failures per hour}$$

$$\lambda_{con} = 50 \times 10^{-9} \times 0.01 = 0.5 \times 10^{-9} \text{ failures per hour}$$

Thus, we can compute the failure rate λ_{sys} of the single network consisting of 32 nodes chained together as:

$$\lambda_{sys} = 40 \times 10^{-9} \times 1 + 50 \times 10^{-9} \times 32 + 0.5 \times 10^{-9} \times (32+1)$$

$$= 1.6565 \times 10^{-6} \text{ failures per hour}$$

Table 2 compares $R_{single}(t)$ and $R_{dual}(t)$ as a function of time ranging from 10 hours to 100,000 hours. The reliability of $R_{dual}(t)$ is always shown to be better than

$R_{single}(t)$. Furthermore, $R_{dual}(t)$ shows a rather good reliability even after the time exceeds 10,000 hours, where $R_{single}(t)$ decreases significantly. Considering the fact that a PCB manufacturing system operates for a few years, the dual network based on IEEE1394 should be used instead of the single one.

Table 2. Comparative table of reliability

hr	10	100	1000	10,000	100,000
Rsingle (t)	0.99998	0.99983	0.99834	0.98357	0.84734
Rdual (t)	0.99999	0.99999	0.99999	0.99973	0.97669

6. Discussion

This paper analyzed the requirements of motion control and arcade games applications, and examined the capabilities of Cyclic-Memory networks based on Ethernet, FDDI, and IEEE1394. According to these analyses and evaluation, the requirement of high bandwidth in both applications can't be satisfied by FL-net and $\mu\Sigma$-100, although they have sufficient segment length, amount of memory, maximum number of nodes attachable to the network, and an acceptable topology except that FL-net lacks memory for arcade games. On the other hand, IEEE1394 shows sufficient performance for both applications and is applicable to motion control, but it is not appropriate for arcade games because it doesn't support the Cyclic Memory. Furthermore, the reliability study of the network based on IEEE1394 for PCB manufacturing has indicated that a dual network is preferred for the usual operating span of the system.

7. References

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